

New FPGA based ARM Development Platform

1. Introduction

Gleichmann Electronics Research, in cooperation with **ARM Cambridge**, is proud to announce the development of a new FPGA based micro controller development platform. The Microcontroller Prototyping Board is based on the Gleichmann **Hpe[®]_midi** platform, an expandable base board with a range of different interfaces. It has a dual FPGA modules for CPU and custom logic implementations and provides peripheral interfaces in a durable enclosure – ideal for software developers. For system prototyping and hardware developers the enclosure can be easily opened to allow rapid access to the expansion ports.



This new system was launched at the ARM Developer's Conference (7th – 9th October 2008 in Santa Clara CA). It retails at \$6,000 including a JTAG control unit and all the tools needed to provide a complete solution for prototyping custom IP around a Cortex-M3 platform.

The **Microcontroller Prototyping Board** is unique as it allows non-licensees of the Cortex-M3 complete access to the core to enable complete customization of the surrounding IP. Key product details include:

- A Cortex-M3 Processor in FPGA
- A complete set of standard, off-the-shelf IP components suitable for system design
- FPGA's to allow full configuration of the supplied components or prototyping of custom IP implementations
- Complete, self-contained physical platform together with graphical tools to configure and program the system
- Supplied with development tools and reference examples

The **Microcontroller Prototyping Board** is the only high-speed system that allows fast, custom system creation with bespoke IP prototyping and comes at a low cost. It can easily be configured and used to model a number of different devices, for example entry level and high-end microcontrollers from the same product family. The high performance means that it's also suitable for benchmarking and software development.

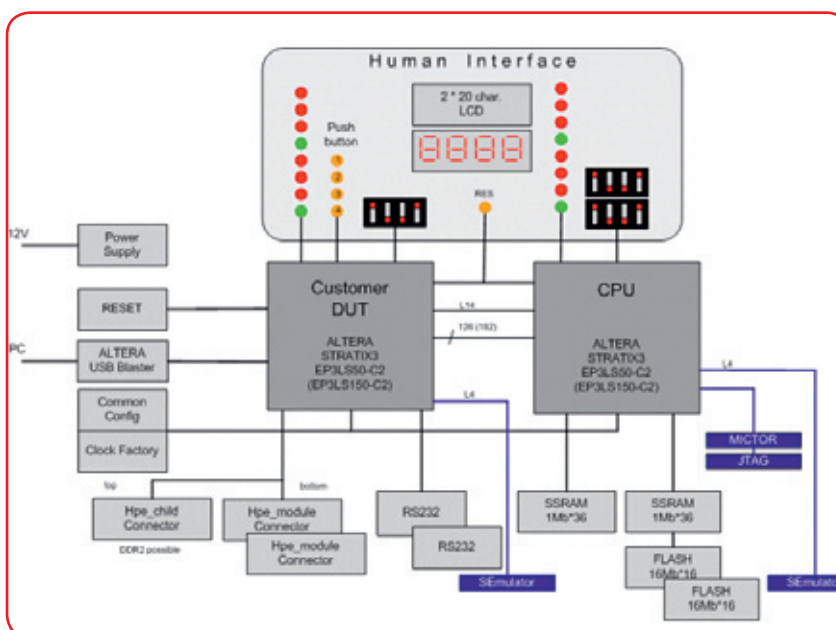
People wishing to design their own microcontroller boards, OEMs interested in specifying their own custom requirements from device vendors, or users interested in performing any sort of Cortex-M3 prototyping are all ideal candidates for this product.

2. Technical Realisation

In conceiving this product we aimed to satisfy a number of key requirements:

- Lowest possible cost
- Highest possible speed
- Maximum availability of physical interfaces on board
- Absolute commitment to quality

The solution: **Hpe®_midiv2** with ARM ALC module



The basic idea of this development kit is to have two FPGAs, one contains the encrypted CPU netlist, the second is free for the user logic. The 2 FPGAs are connected via an AMBA-bus lite interface together with some additional free channels.

The system is designed to accommodate different CPUs, including forthcoming ARM designs, so customers can customize their solution. Also updates or patches can be easily delivered by email.

For the DUT FPGA Gleichmann Research offers a library of standard IP components from a range of international IP providers – together with an automatic connecting tool. This minimizes the configuration overheads for the system developer, shortening development time and increasing design quality.

Below is a detailed description of the components of the module and the physical interfaces of the base board.

2.1 Components on the module

CPU FPGA:	ALTERA Stratix3® EP3SL50-C2
Customer DUT FPGA:	ALTERA Stratix3® EP3SL50-C2 or EP3SL150-C2
System RAM:	2 * 2 MB SSRAM
Program Flash:	512 MB Flash
Programming Device:	Original ALTERA USB Blaster®
FPGA Config:	Parallel Flash
Serial I/F:	2 * RS232
Different connectors:	20 pin flat ribbon for debug tools MICTOR for debug tools 2 * SEmulator connector (explanation later) 1 * Hpe®_child board connector 2 * Module connector, connection to base board
Human interface:	5 push button 3 * 4bit DIP switch 16 LED 4 digit 7 segment display LCD connector with 2*20 character LCD in the front panel

2.2 Components on the base board

2 * RS232	1 * AC97
1 * Ethernet 10/100	1 * TFT with touch
1 * CAN	4 * 12 bit D/A (Cypress PSOC)
1 * LIN	4 * 12 bit A/D (Cypress PSOC)
1 * FlexRay	DVI-I
2 * USB Host (NXP1761)	SD-Card
1 * USB Target	

3. Development Support

All ARM development platforms which are based on the **Hpe®_midi** system, will be supplied with a complete set of tools to assist the developer during the design process. The tools have been developed to allow complete integration between hardware and software development. Supplying the best software tools ensures the maximum potential can be realised from excellent hardware. The Gleichmann Hpe® tools (Hardware Prototype and Emulation) guarantees this close collaboration between hardware and software.

In the following chapters we introduce new tools for the development for an ARM based development. As well as the tools supplied there is a range of compatible tools from ARM and other 3rd party vendors.

3.1 Hpe®_desk

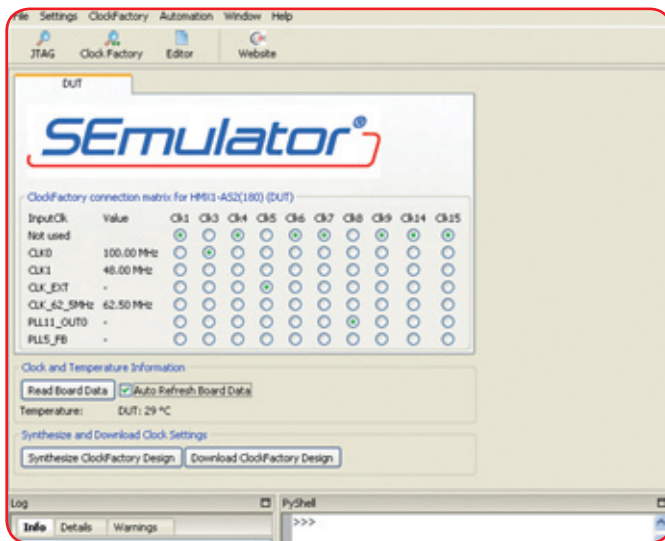
The Hpe®_desk is the overall GUI which supports the following tools:

- Clock factory
- Hpe® JTAG
- Hpe®_AIM
- SEmulator with associated functions

3.2 Clock factory

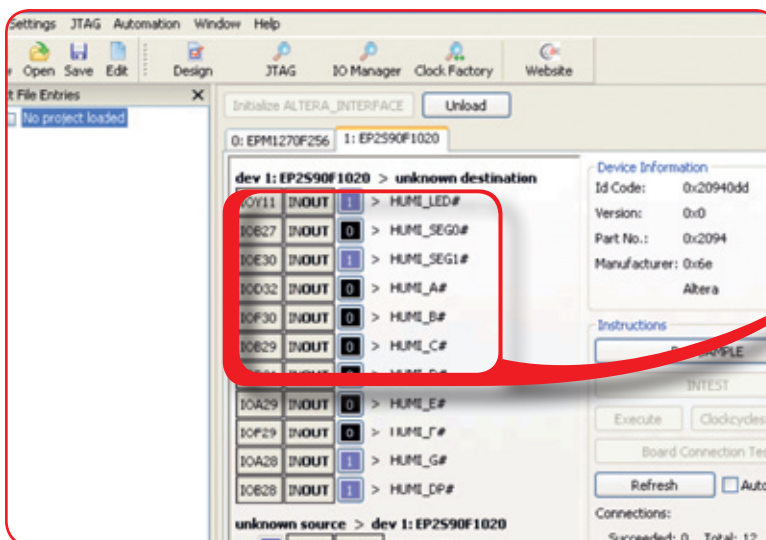
The **Hpe®_midi** supports various clock sources. One quartz based system frequency, two oscillator sockets, two PLL outputs from FPGA and one external clock via SMA connector. These clocks can be routed to up to 16 clock inputs of the FPGA. The wiring is done in a CPLD. The user needs no special knowledge of the actual hardware as there is a graphical interface with an easily selectable matrix which automatically handles the synthesis and programming of the CPLD.

The junction temperature of both FPGAs is also displayed.



3.3 Hpe®_JTAG

Hpe®_JTAG is a tool for interactive PCB debugging. It comes free of charge with every **Hpe®_midi** system. **Hpe®_JTAG** provides a graphic user interface, but also powerful Python-scripting capabilities. The screenshot below shows an example for a scan chain containing two JTAG compatible devices that are represented by the two tabs.



IO-Filtering:
Observe IOs of interest only

Pin-File parsing:
Use your HDL top-level pin names to find signals

Instead of graphically representing exhaustive grid arrays, each with over a thousand IOs, a filter function allows the user to display only IO's that are currently of interest.

Hpe®_JTAG supports the following JTAG instructions:

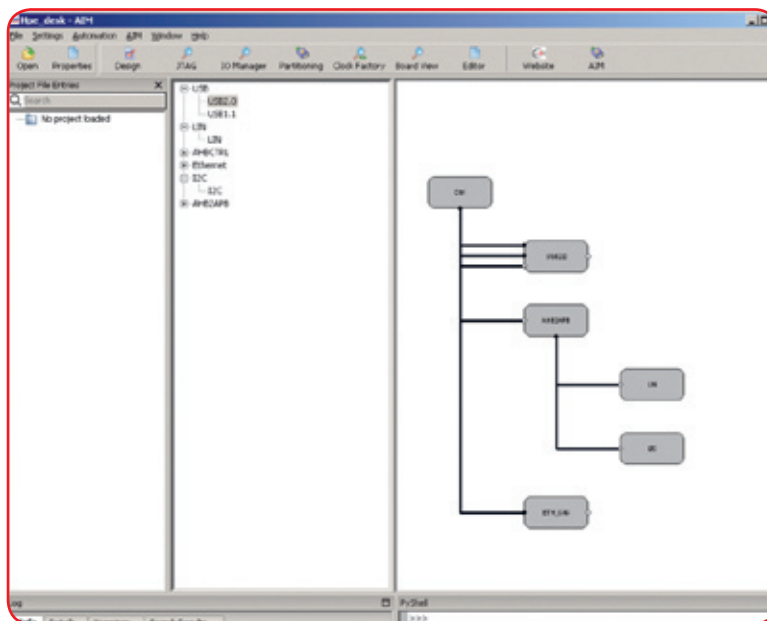
- **SAMPLE:** The SAMPLE instruction is used to get a snapshot of the current pin states of a device in the JTAG chain. It is unintrusive and does not influence the device operation.
- **EXTEST:** The EXTEST instruction is used to check a connection between devices in one JTAG chain. The values of output pins can be set and the values of input pins can be read.
- **INTEST:** The INTEST instruction is used to check the internal functionality of a device in the JTAG chain. The values of input pins can be set and the values of output pins can be read. Note that the availability of the INTEST instruction depends on the devices' capabilities.

3.4 Hpe®_AIM
(AMBA IP Manager)

The system is supplied with sets of IP from a range of IP providers including ARM. These IP blocks offer a modular set of functions which enables the user quickly and easily build a fully integrated bespoke system. Gleichmann Research only adds certified macros to this library.

This certification includes the following:

- Availability of a demonstration design, which developers can use for reference
- Functional check of IP in standard configurations
- Availability of test pattern
- Datasheet and description
- Basic and detailed pricing information



The working window of the **Hpe®_AIM** consists of 5 different panes. Key areas of interest are the top right and middle panes. The middle pane shows all currently installed macros. The user can drag and drop every IP component to the top right window, where it is automatically connected to the bus system. The user can then modify the generic parameters of the component by right clicking the block. If the IP is only available as netlist only the AHB address and mask are configurable. Contextual tooltips give instant information about the characteristics of each of the IP blocks (e.g. vendor, price, size).

Drag and drop operations are supported for fast and easy configuration.

3 groups of IP are available:

- Bus Interface e.g. AHBlite2AHB, AHBlite2APB, AHB2AHB, AHB2APB
- AHB bus IP e.g. Ethernet, display controller, video controller
- APB bus IP e.g. UART, I2C, GPIO

Once all IP components are configured the tools automatically generate a netlist, synthesizes it and transfers the bit stream into the FPGA. Custom IP can also be easily implemented with the **Hpe[®]_AIM**.

Licensing of IP components can be done directly with the IP provider or, if IP is required from several different providers Gleichmann Research can do this by request. The IP components are delivered on a DVD supplied with the hardware.

They can also be downloaded from the ALTERA and Gleichmann Electronics Research web site. The tool is supplied free of charge with the **Hpe[®]_midi** system.

3.5 SEmulator[®] *SEmulator[®]*

The SEmulator[®] is a tool which helps the developer to increase speed and quality of the design process. The hardware offers a high speed link of 2,5 Gbit/s between the PC and each FPGA. The S2-Box contains a PCI Express X4 over cable input and a connection for 2 FPGAs via L4 interfaces. Highlights of the SEmulator[®] include:

- **Hardware Acceleration:** The FPGA can be used as accelerator for Mentor ModelSim or ALDEC ActiveHDL simulator. Simulation speed-up of up to 600 times possible. (10 hour simulation time drops to 1 minute!)
- **Hardware in the Loop:** Every real hardware component on the module, base board or any child board can be used as an actual simulation model, as well as the CPU in the FPGA
- **Logic Analyzer:** Based on ALTERA's signal tap, but using data storage on the PC rather than the FPGA giving superior storage capacity.
- **Hardware Fault Injector:** STUCK@, pulse, multiple pulses, SEU, MEU combined with the acceleration and benefits of analysis software.
- **CPU Debugger:** Currently in development.

You will find detailed information about these tools under www.ge-research.com.

Authors

Alex Growcoot
ARM Limited
110 Fulbourn Road
Cambridge
CB1 9NJ
United Kingdom

Dieter Scheurer
Gleichmann Electronics Research
Softwarepark 37
4232 Hagenberg
Austria



Gleichmann Electronics Research (Austria) GmbH & Co KG

Softwarepark 37 • A-4232 Hagenberg
Tel: +43 7236 3351 4500 • Mail: sales@ge-research.com
www.ge-research.com