

SEmulator® Turbo Charging for FPGA-Designs

Faster and more secure to “Working Silicon”

- Early and continued testing of final hardware ▶ Higher design quality / reliability
- Dramatically decrease RTL simulation time ▶ Decrease development time
- Standard FPGA board for development ▶ Minimum additional hardware cost
- Hardware in the Loop ▶ Every external hardware can be implemented easily in the **SEmulator®**
- ‘No’ limitation on pin and gate count ▶ Broad family concept – Many extension boards

SEmulation: The principle

Our **SEmulator®** gives the engineer the possibility to run the simulation on real hardware.

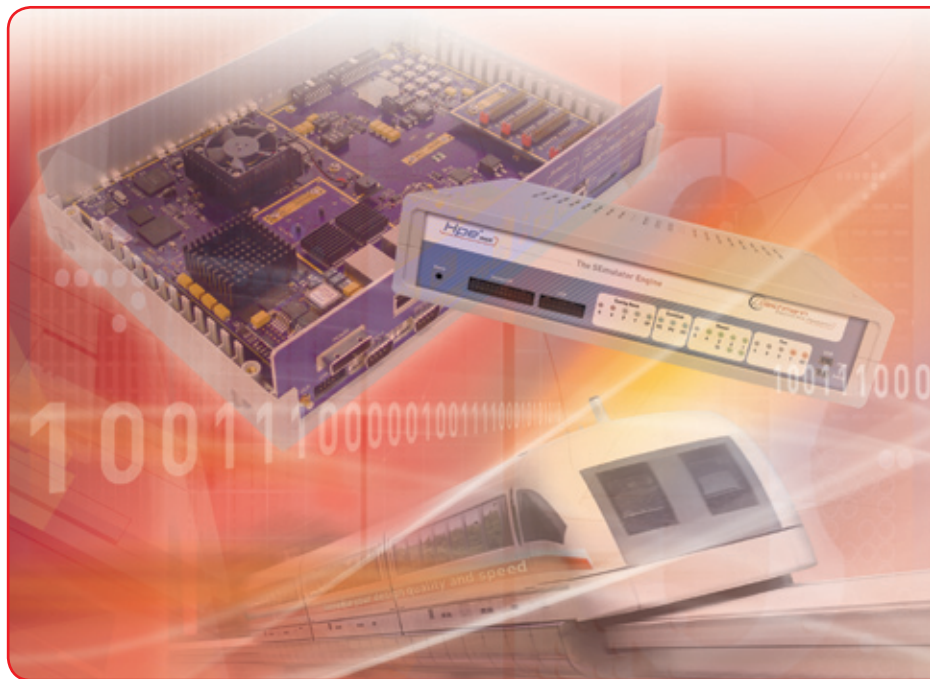
Simulation and complete functional verification of the final silicon takes place in a single test environment.

After the first simulation, function tested macros will be transferred into the target hardware one by one.

Next simulations integrate the emulation of the external macros.

After the assignment of all macros in the FPGA, simulator controlled hardware emulation takes place.

That's SEmulation.



SEmulation: The convenience

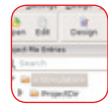
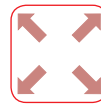
- Working with the used development environment the simulation duration shortens and so the whole development time will be shorter as well.
- The effort of smaller modifications of existing systems will be reduced dramatically. This reduces not only the costs, but also leads to increased reactivity on market requirements.
- Mistakes and insecurities are eliminated, as there are no differences between simulation environment and target hardware.
- The unerring development results in functional “First Silicon” and therefore leads to a reduction of development costs.
- Due to reduced investment costs, all companies can use SEmulation.

Our Start-up Package = 19.890 Euro

- Hpe_midi with 1 FPGA module (EP2S180)
- PCI Express Bundle
- SEmulator® Software
- ALDEC “Active HDL” Simulator

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Gleichmann Research offers a complete concerted development platform with innovative high quality FPGA development boards and a set of software tools to support the developer.

The times are gone where the developer has to evaluate a different set of tools for each FPGA family, which costs time and money and still these are not perfect.



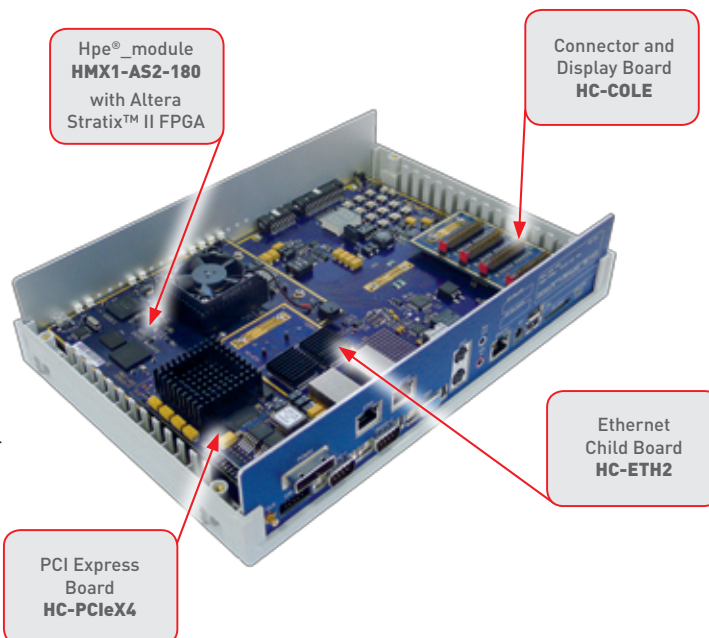
Based on the ALTERA® EP2S180 in a 1508 pin package, Gleichmann Research offers a 2-FPGA-module for the **Hpe®_midi** systems.

Every FPGA has 180.000 logic elements (equivalent to 1.8 Mio. ASIC gate). There are 700 interconnections between the FPGA's, 64 LVDS pairs allow 1Gbit/s/pair high-speed data communication.

A 24-layer PCB, impedance controlled, temperature depended fan control and a clock factory, which distribute 7 input clocks to different clock inputs of the FPGA's – these are some of the features of our FPGA development systems. We have also implemented the ALTERA® USB-Blaster™ on the module.



The **Hpe®_midi** can be used closed from software developer. The hardware developer can use it open with the direct contact and access to the hardware. Many child boards help you to start very fast from the scratch. If you order a child board you will get a customer specific rear panel without any additional charge.



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